substantially the same structure, however, the gate insulation film just under the selective gate electrode 18a is formed thicker than the memory transistor area. Further, the selective gate electrode 18a is connected to the second gate electrode 16b of the floating gate electrode 16 which is consecutively formed in pattern without being isolated in the direction of the word line, in a proper position excluding a sectional position in FIG. 4B.

(9) In this embodiment, as shown in the section in FIG. 4A, an upper edge corner A of the element isolation insulation film 14 is recessed by isotropic etching, and terminates at a side surface of the first gate electrode 16a of the floating gate electrode 16.

(10) That is, a position of the surface coming into contact with the floating gate electrode 16 at the corner A is lower than an upper surface of the first gate electrode 16a but higher than an interface with the gate insulation film 15. Further, in an area disposed away from the corner A, the surface position of the element isolation insulation film 14 is higher than that of the first gate electrode 16a.

(11) Next, a process of manufacturing the NAND type memory array described above, will be specifically explained. FIGS. 5A-5H show the manufacturing process thereof of the section in FIG. 4A.

(12) As shown in FIG. 5A, a gate insulation film 15 is formed on a silicon substrate 11, and a first gate electrode 16a which will serve as a floating gate electrode is deposited on the gate insulation film 15. Then a silicon nitride layer 31 serving as a stopper mask material when in a CMP process of the element isolation insulation film, is further deposited on the first gate electrode 16a. In this embodiment, the gate insulation film 15 is defined as a tunnel oxide layer formed by thermal oxidation. Furthermore, the gate electrode 16a is an amorphous silicon layer or a polycrystalline silicon layer.

(13) A resist pattern 32, of which an opening is formed in the element

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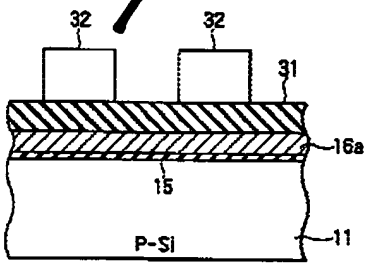

FIG. 5A

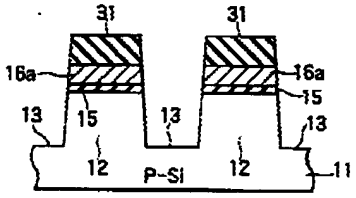

FIG. 5B

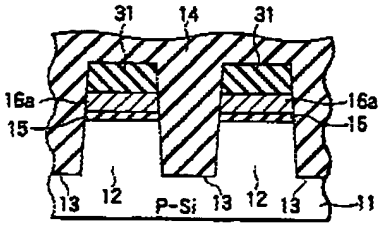

FIG. 5C

Col 6 see lines 33-43 polish-stop etch 48-57

US006222225B1

(12) **United States Patent**
Nakamura et al.

(10) **Patent No.: US 6,222,225 B1**
(45) **Date of Patent: Apr. 24, 2001**

(54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF**

(75) Inventors: Takuya Nakamura, Kanagawa-Ken; Naoki Kishi; Hirohito Iizuka, both of Yokohama; Kazuhito Narita, Yokosuka; Seiichi Aritsuka, Yokohama; Fumitaka Arai, Isogo-Ku, all of (JP)

(73) Assignee: Kabushiki Kaisha Toshiba, Kawasaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/400,856

(22) Filed: Sep. 27, 1999

(30) Foreign Application Priority Data

Sep. 29, 1998 (JP) 10-276126
Sep. 9, 1999 (JP) 11-255165

(51) Int. Cl.[7] H01L 29/788

(52) U.S. Cl. 257/316; 257/374; 257/506; 257/510

(58) Field of Search 438/296, 297, 455/434, 435, 257/239, 251, 230, 374, 501, 502, 510, 514, 521, 315, 321

(56) References Cited

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6,036,365 * 3/2000 Sakimoto et al. 257/315
6,069,053 * 5/2000 Ueda et al. 438/439

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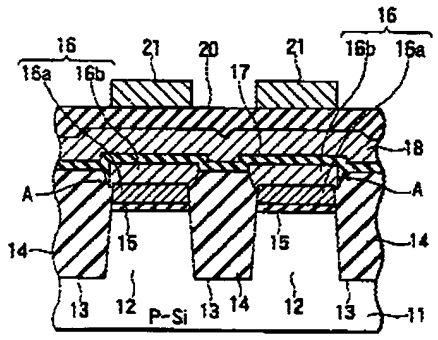
Primary Examiner—Olik Chaudhuri
Assistant Examiner—Hoai Pham
(74) *Attorney, Agent, or Firm*—Banner & Witcoff, Ltd.

(57) **ABSTRACT**

A semiconductor device has a semiconductor substrate, an element isolation insulation film embedded in a trench formed in said semiconductor substrate in a state of protruding from a surface of said semiconductor substrate and a transistor having a gate electrode provided in an area surrounded by said element isolation insulation film on said semiconductor substrate, and containing a gate electrode deposited through a gate insulation film before embedding said element isolation insulating film and an upper edge corner of said element isolation insulation film is selectively recessed. In the thus structured semiconductor device, the upper edge corner of the element isolation insulation film is recessed before the patterning process of the gate electrode, thereby preventing such a situation that a part of the gate electrode remains unetched in the patterning process of the gate electrode.

9 Claims, 13 Drawing Sheets



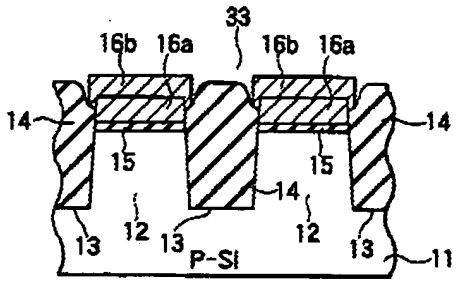


FIG. 5G

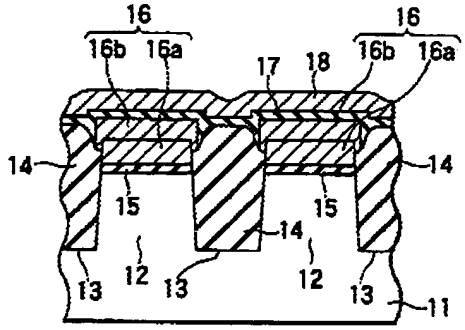


FIG. 5H

US006222225B1

(12) **United States Patent**
Nakamura et al.

(10) **Patent No.: US 6,222,225 B1**
(45) **Date of Patent: Apr. 24, 2001**

(54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF**

(75) Inventors: Takuya Nakamura, Kanagawa-Ken; Naoki Kishi; Hirohito Iizuka, both of Yokohama; Kazuhito Narita, Yokkaichi; Satoshi Arikuma, Yokohama; Fumitaka Arai, Inagi-Ku, all of (JP)

(73) Assignee: Kabushiki Kaisha Toshiba, Kawasaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/408,858

(22) Filed: Sep. 27, 1999

(30) **Foreign Application Priority Data**

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Sep. 8, 1999 (JP) 11-253161

(51) Int. Cl.[7] H01L 29/788

(52) U.S. Cl. 257/316; 257/374; 257/906; 257/510

(58) Field of Search 438/296, 297, 455/514, 439, 257/239, 211, 230, 374, 901, 906, 510, 514, 521, 315, 321

(56) **References Cited**

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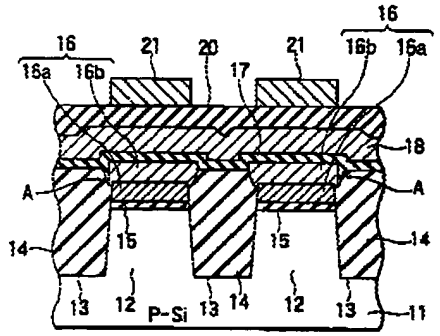
Primary Examiner—Olik Chaudhuri
Assistant Examiner—Hoai Pham
(74) *Attorney, Agent, or Firm*—Banner & Witcoff, Ltd.

(57) **ABSTRACT**

A semiconductor device has a semiconductor substrate, an element isolation insulation film embedded in a trench formed in said semiconductor substrate in a state of protruding from a surface of said semiconductor substrate and a trench having a gate electrode provided in an area surrounded by said element isolation insulation film on said semiconductor substrate, and containing a gate electrode deposited through a gate insulation film before embedding said element isolation insulation film and an upper edge corner of said element isolation insulation film is selectively recessed. In the thus structured semiconductor device, the upper edge corner of the element isolation insulation film is recessed before the patterning process of the gate electrode, thereby preventing such a situation that a part of the gate electrode remains unetched in the patterning process of the gate electrode.

9 Claims, 15 Drawing Sheets



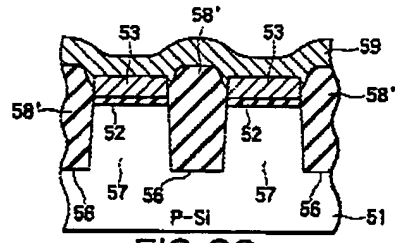


FIG. 9G

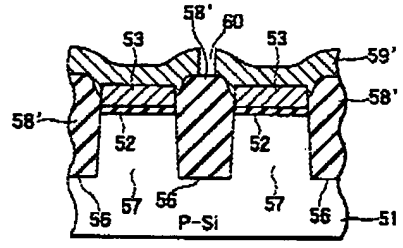


FIG. 9H

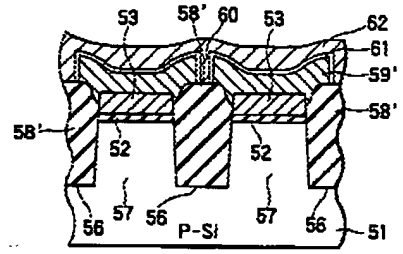


FIG. 9I

of the cell. The voltage on the control gate is capacitively coupled to the floating gate, so a potential difference appears between the floating gate and the source, drain or channel region. This potential difference is used to change the charge on the floating gate.

(4) In order to reduce the potential difference that has to be provided between the control gate and the source, drain or channel region, it is desirable to increase the capacitance between the control and floating gates relative to the capacitance between the floating gate and the source, drain or channel region. More particularly, it is desirable to increase the "gate coupling ratio" GCR defined as CCG/(CCG+CSDC) where CCG is the capacitance between the control and floating gates and CSDC is the capacitance between the floating gate and the source, drain or channel region. One method for increasing this ratio is to form spacers on the floating gate. See U.S. Pat. No. 6,200,856 issued Mar. 13, 2001 to Chen, entitled "Method of Fabricating Self-Aligned Stacked Gate Flash Memory Cell", incorporated herein by reference. In that patent, the memory is fabricated as follows. Silicon substrate 104 (FIG. 1) is oxidized to form a pad oxide layer 110. Silicon nitride 120 is formed on oxide 110 and patterned to define isolation trenches 130. Oxide 110 and substrate 104 are etched, and the trenches are formed. Dielectric 210 (FIG. 2), for example, borophosphosilicate glass, is deposited over the structure to fill the trenches, and is planarized by chemical mechanical polishing (CMP). The top surface of dielectric 210 becomes even with the top surface of nitride 120. Then nitride 120 is removed (FIG. 3). Oxide 110 is also removed, and gate oxide 310 is thermally grown on substrate 104 between the isolation trenches. Doped polysilicon layer 410.1 (FIG. 4) is deposited over the structure to fill the recessed areas between the isolation regions 210. Layer 410.1 is polished by chemical mechanical polishing so that the top surface of layer 410.1 becomes even with the top surface of dielectric 210.

(5) Dielectric 210 is etched to partially expose the "edges" of polysilicon layer 410.1 (FIG. 5). Then doped polysilicon 410.2 (FIG. 6) is deposited and etched anisotropically to form spacers on the edges of polysilicon 410.1. Layers 410.1, 410.2 provide the floating gates.

(6) As shown in FIG. 7, dielectric 710 (oxide/nitride/oxide) is formed on polysilicon 410.1, 410.2. Doped polysilicon layer 720 is deposited on

Ding

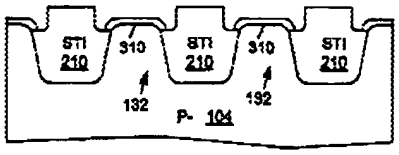


FIG. 13

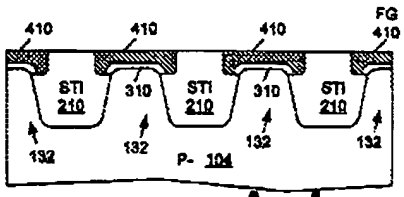


FIG. 14

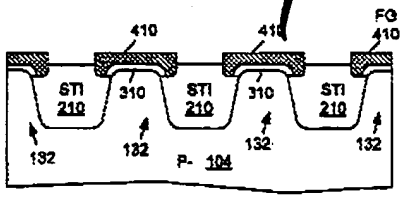


FIG. 15

Col 1, L35-55

Col 3 L30-40